國立臺北科技大學 材料及資源工程系

矽奈米元件物理
SILICON NANOMETER DEVICES AND PHYSICS

Introduction to Semiconductor

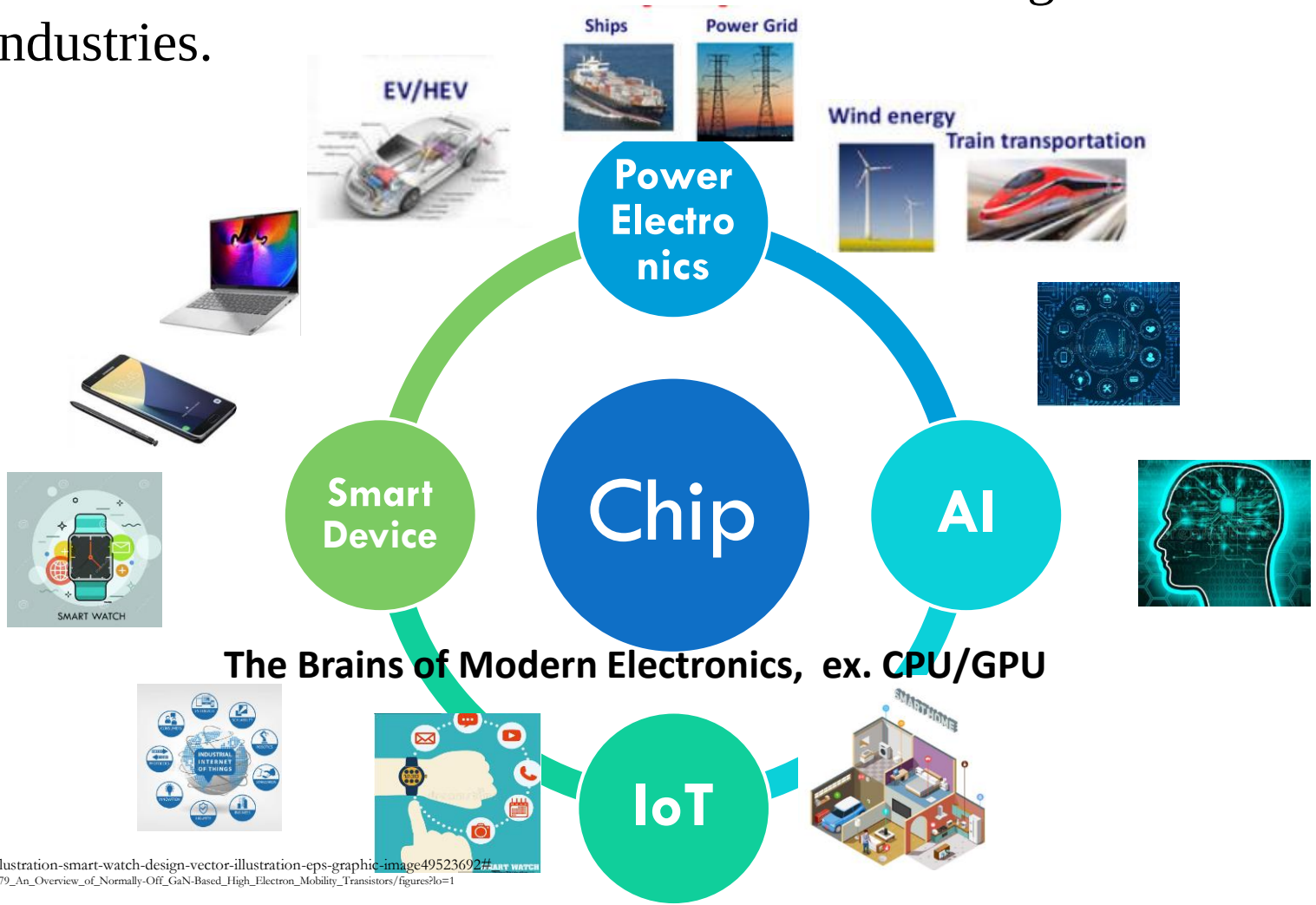
徐曉萱

Outline

- **Introduction to the Semiconductor**
- How does Semiconductor Work?
- Si Wafer Orientation

What is a Semiconductor?

- Semiconductor is the core material for modern Integrated Circuit (IC) industries.



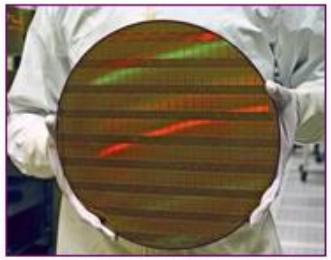
From: Samsung

https://www.dreamstime.com/stock-illustration-smart-watch-design-vector-illustration-eps-graphic-image49523692#

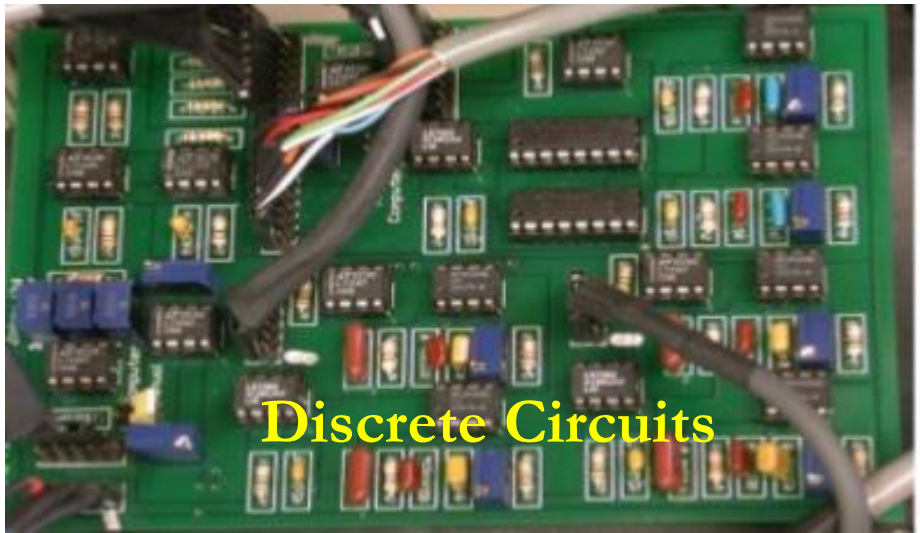
https://www.researchgate.net/publication/333119779_An_Overview_of_Normally-Off_GaN-Based_High_Electron_Mobility_Transistors/figures?lo=1

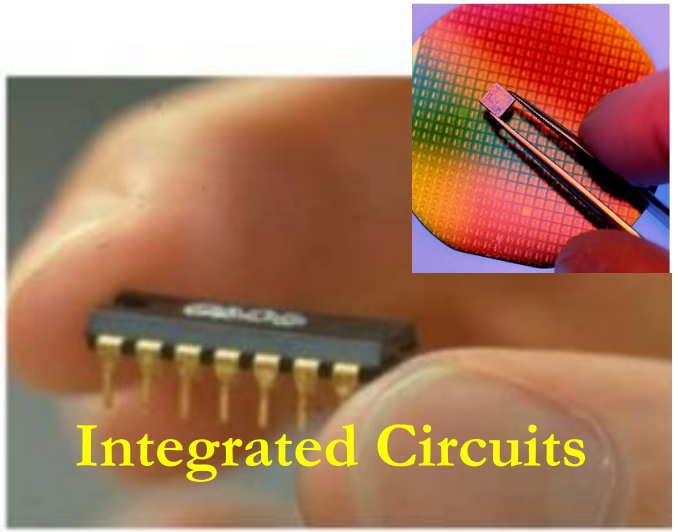
Integrated Circuit (IC) 積體電路

- An integrated circuit (IC) is a set of electronic devices on the top of a small flat Silicon(Si) wafer.
  - ✓Many transistors on one **chip**.
  - ✓Less power consumption being small in size.
  - ✓No soldering. Good reliability & performance.
  - ✓Handling limited power



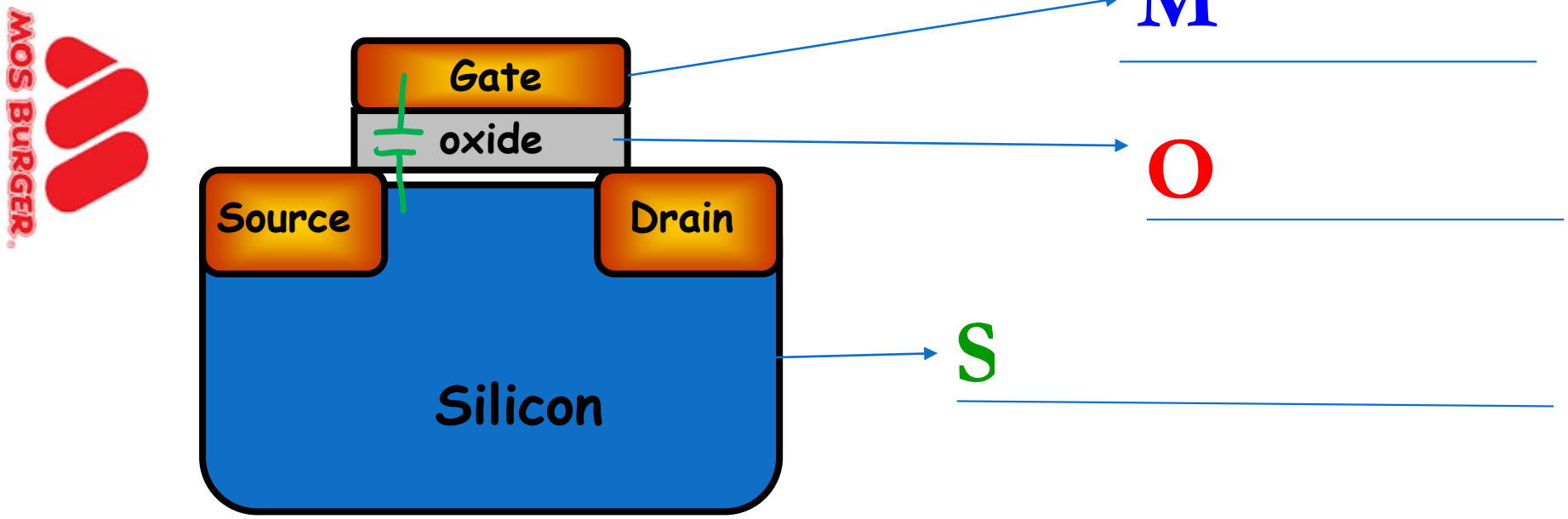
Intel®300 mm wafer with 45 nm shuttle test chips





MOS Transistor (MOSFET)

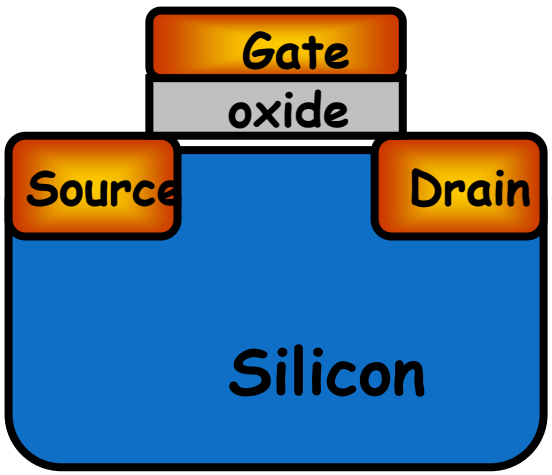
MOSFET=MOS Field-Effect Transistor

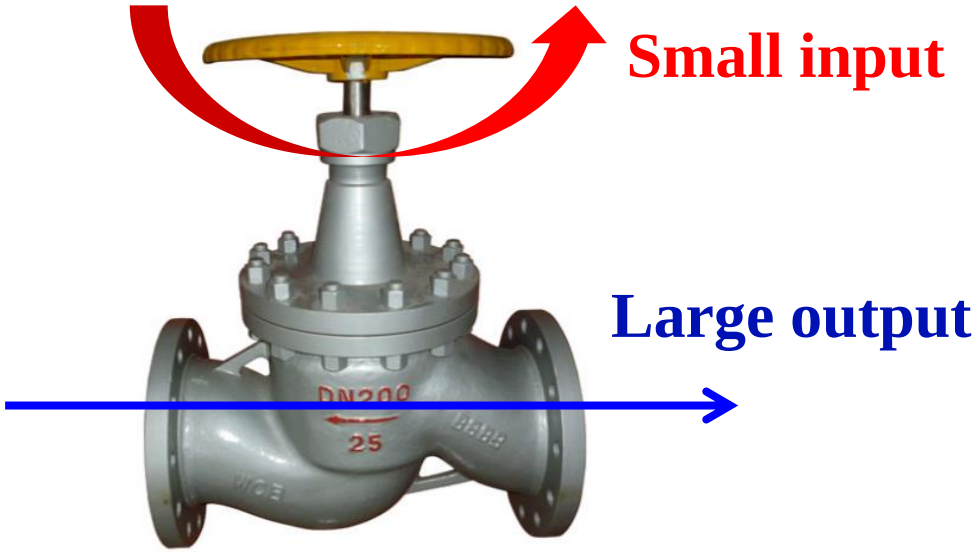


- "Transistor" is a combination of the terms "transconductance" and "variable resistor".
- A transistor is a 3 terminal electronic device made of semiconductor material.

What is a MOS transistor (MOSFET)?

- Transistors have the ability to behave as an electrically controlled on/off switch to perform the foundational logical computations in a computer.
- Transistors have many uses, including amplification, switching, voltage regulation, and the modulation of signals.





What is a Semiconductor?

- Semiconductors are materials with electrical conductivity ($\boldsymbol{\sigma}$) caused by the flow of free electrons or holes.
  - ✓With free electrons/holes and external stimulation (_____), semiconductors are conductors and current can be generated.
  - ✓Without free electrons/hole and external stimulation, semiconductors are insulators.

- To introduce more electrons or holes, a technique called ‘doping’ is required.

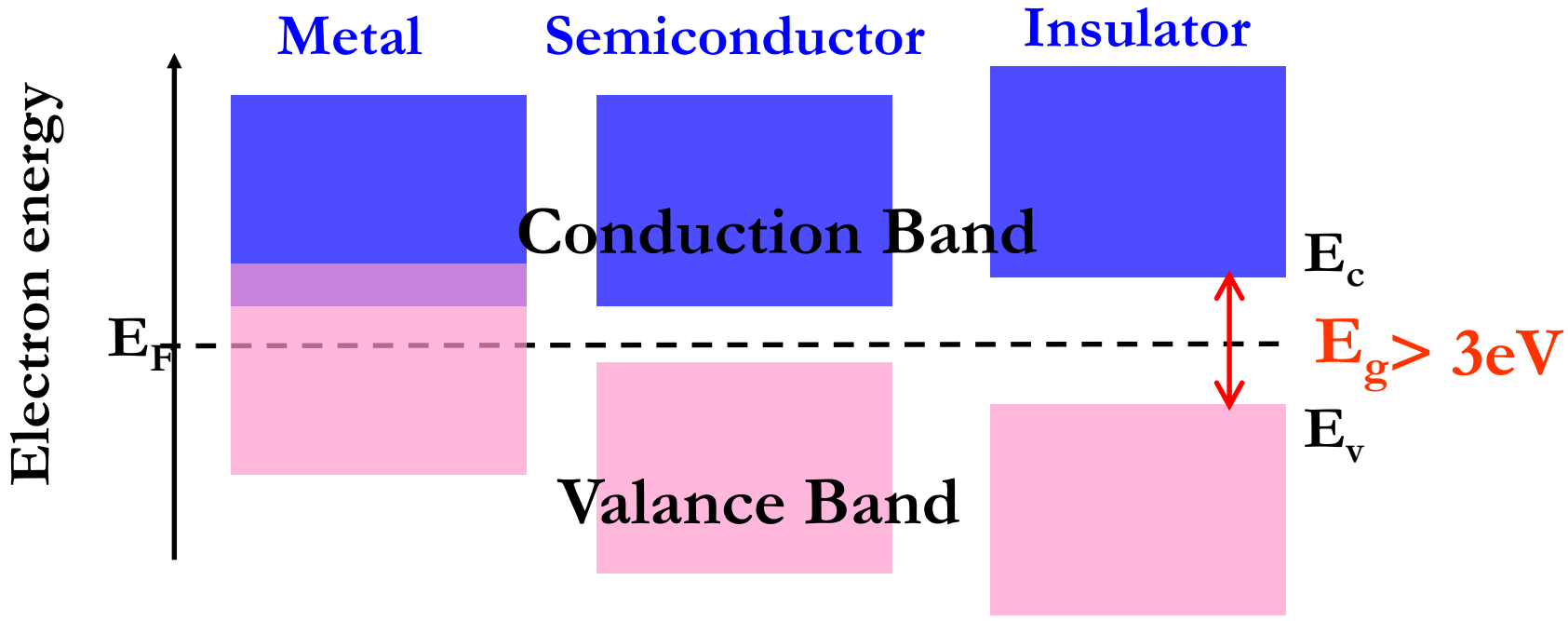
Classification of Material

***Electrical Conductivity*: σ $(\Omega\text{-m})^{-1}$**

METALS	conductors	CERAMICS	
Silver	6.8×10^{7}	Soda-lime glass	10^{-10}-10^{-11}
Copper	6.0×10^{7}	Concrete	10^{-9}
Iron	1.0×10^{7}	Aluminum oxide	$<10^{-13}$
SEMICONDUCTORS		POLYMERS	
Silicon	4×10^{-4}	Polystyrene	$<10^{-14}$
Germanium	2×10^{0}	Polyethylene	10^{-15}-10^{-17}
GaAs	10^{-6}		
	semiconductors		insulators

Selected values from *Callister 7e*.

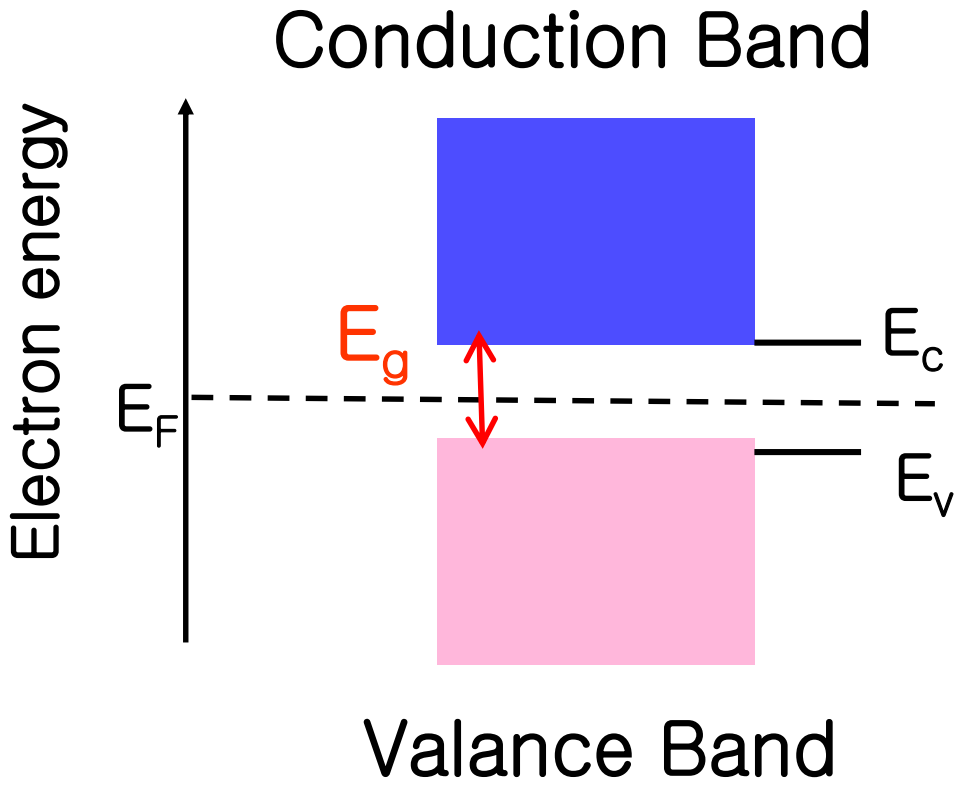
Energy Band Diagram (E,x)



4A

Element	Atomic number	Band gap (eV) E_g		Melting point (°C)
Carbon	6	5.30	Insulator	3800
Silicon	14	1.12		1417
Germanium	32	0.66	Semiconductor	937
Tin (α–Sn)	50	0.08	Metal	232

Definition of Energy Bands



Fermi energy (E_F) :
energy of the highest filled state at 0 K

- **Valence band** (filled): highest occupied energy levels at **0 K**, Ev
- **Conduction band** (empty):lowest unoccupied energy levels, Ec

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- Introduction to the Semiconductor
- **How does Semiconductor Work?**
- Si Wafer Orientation

Semiconductors Types

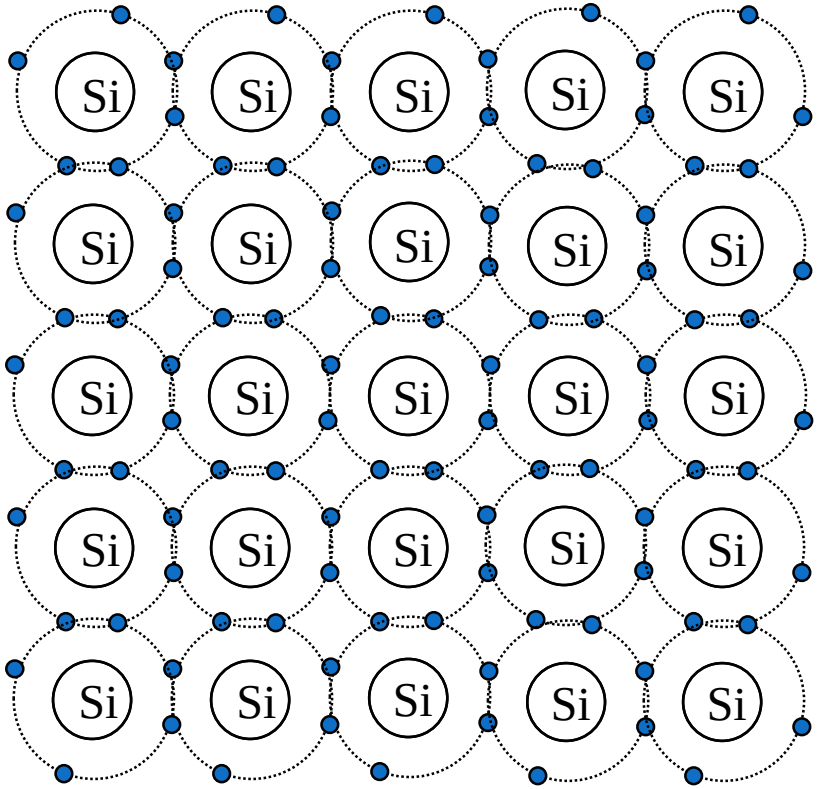
- **Intrinsic semiconductors:**
  - ✓ Pure material, no intentional impurities.
  - ✓ Number of electrons = Number of holes (***n*** = ***p***)
  - ✓ Relatively high resistivity.

- **Extrinsic semiconductors:**
  - ✓ Intentional addition of controlled amounts of specific atoms to enhance the conductivity by changing the carrier concentrations.
  - ✓ When we add impurities to semiconductors, we call the impurities as **dopants** and the process is called **doping.**

Elements Used in Semiconductor

Acceptor Dopant		Semiconductor		Donor Dopant	
Group 3 (p-type)		**Group 4**		**Group 5 (n-type)**	
Boron (B)	**5**	Carbon	6	Nitrogen	7
Aluminum	13	**Silicon (Si)**	**14**	**Phosphorus (P)**	**15**
Gallium	31	Germanium	32	**Arsenic (As)**	**33**
Indium	49	Tin	50	**Antimony (Sb)**	**51**

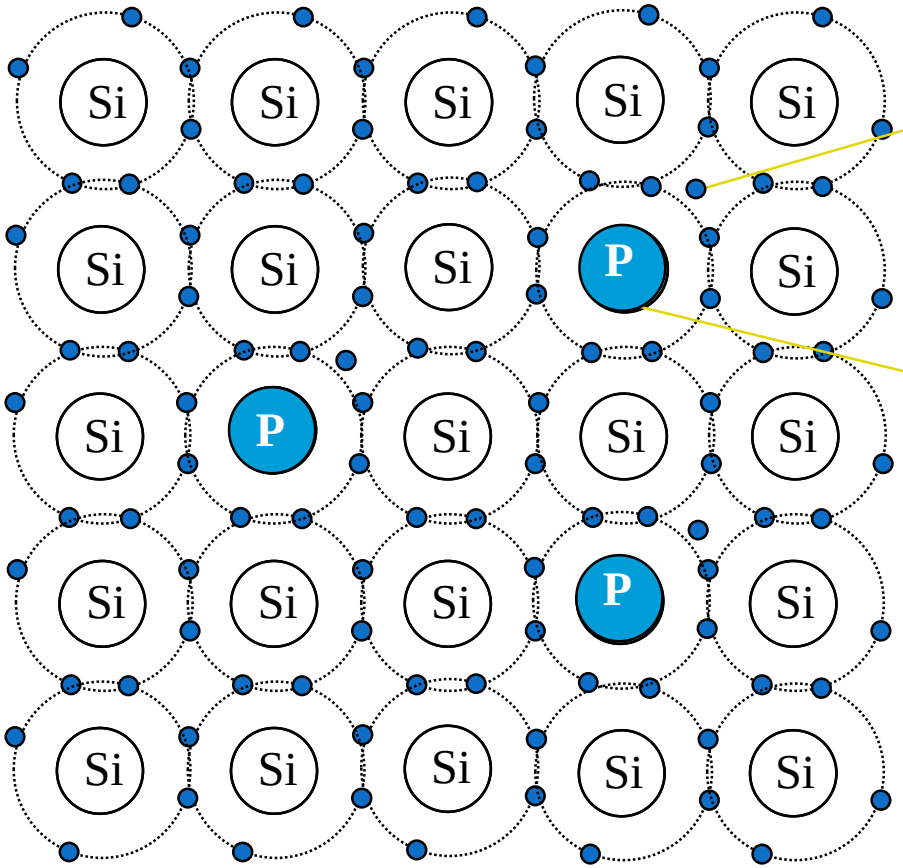
Covalent Bonds in Silicon Crystal



Silicon atoms share valence electrons to form insulator-like bonds

Free Electrons (e^-) in n-type Si

Donor atoms (5A element) provide excess electrons to form n-type Si.

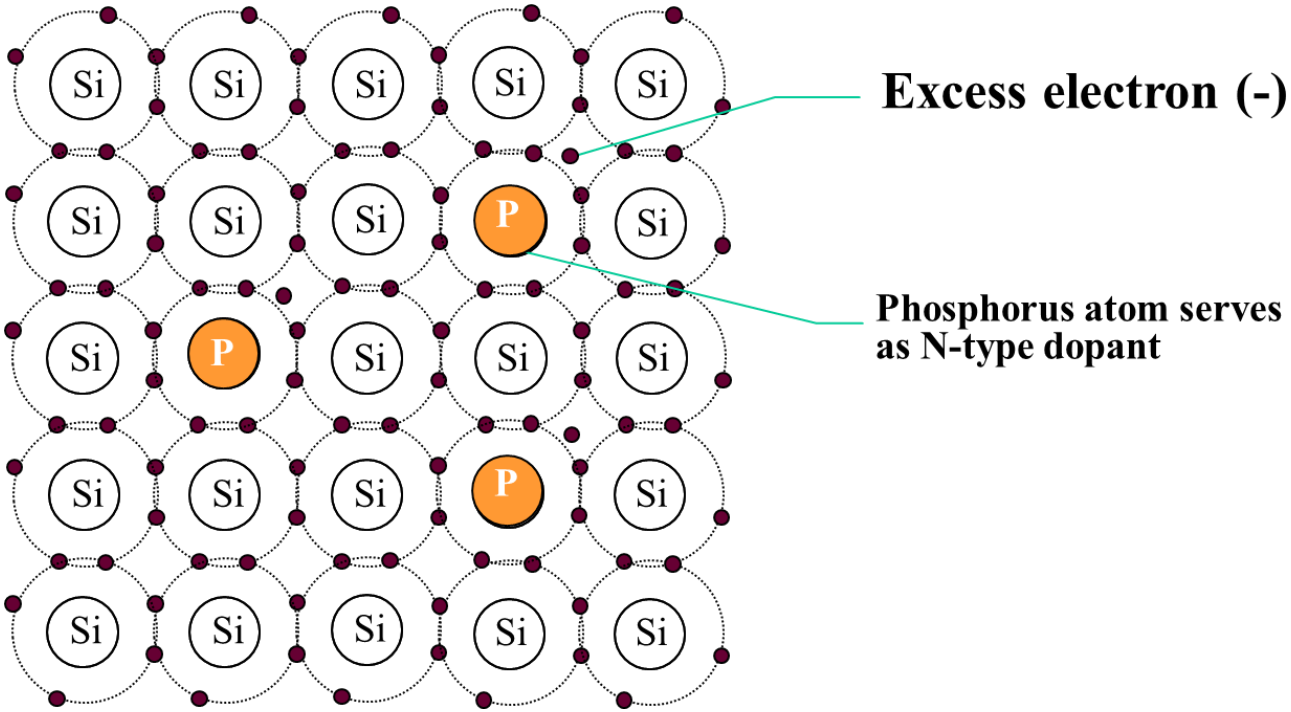


Excess electron (-)

Phosphorus atom serves as N-type dopant

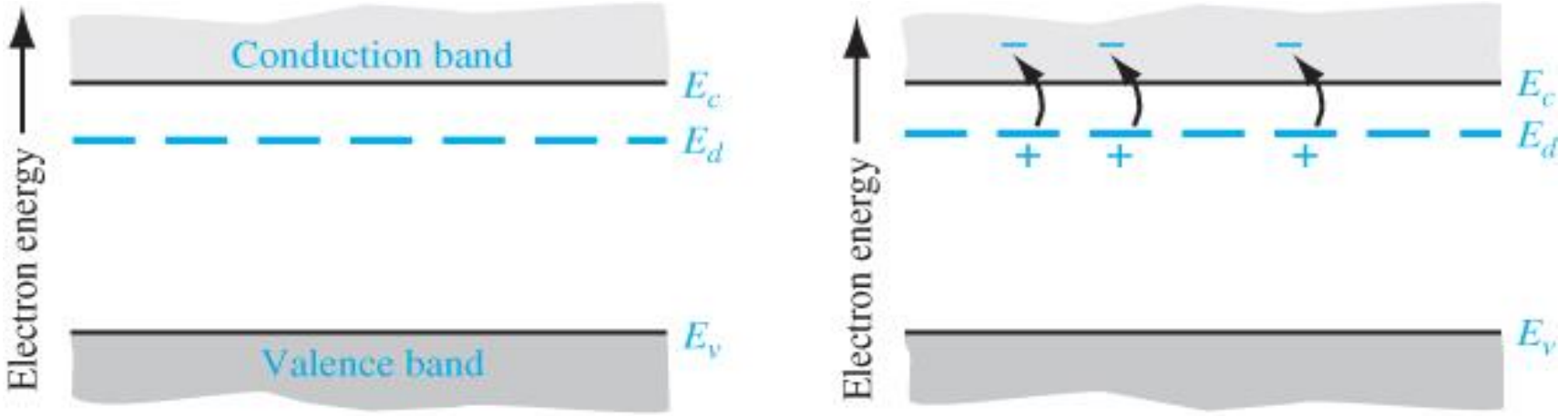
Free Electrons in n-type Si

- A group V element, such as P atom is added into Si. 4 of valence electrons contribute to the covalent bonding, leaving the 5th electron loosely bound (~0.05 eV) to P atom, referred as a donor electron.
- Donor atoms provide excess electrons to form N-type silicon.



Free Electrons in n-type Si

- The energy level E_d is the **energy state of donor impurity**.
- If a small amount of energy, such as thermal energy, is added to the donor electron, it can be elevated into CB, leaving behind a positively charged P ion.
- **Donor atoms** can add electrons to contribute the CB current, without creating holes in VB.

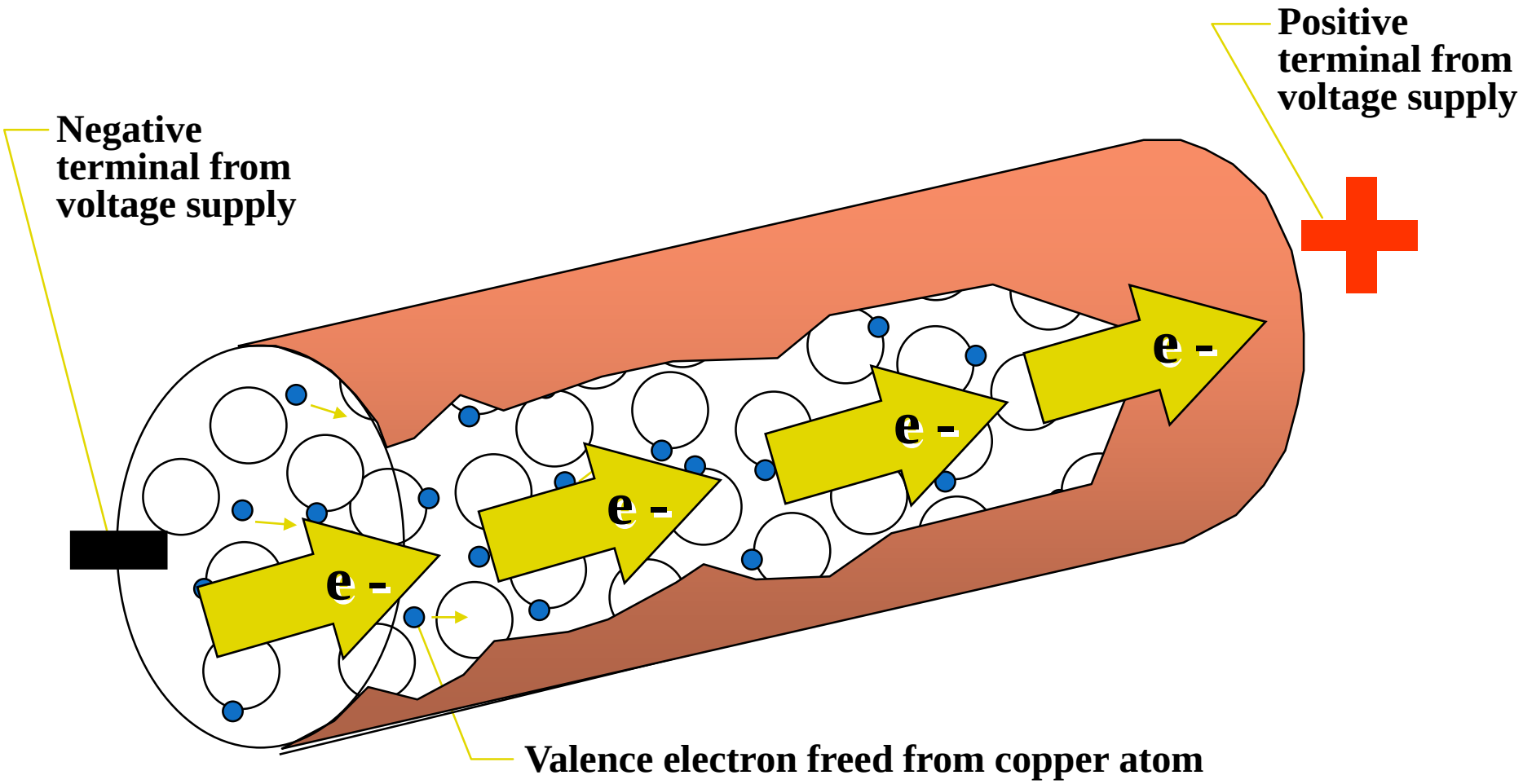


n-Type Semiconductor

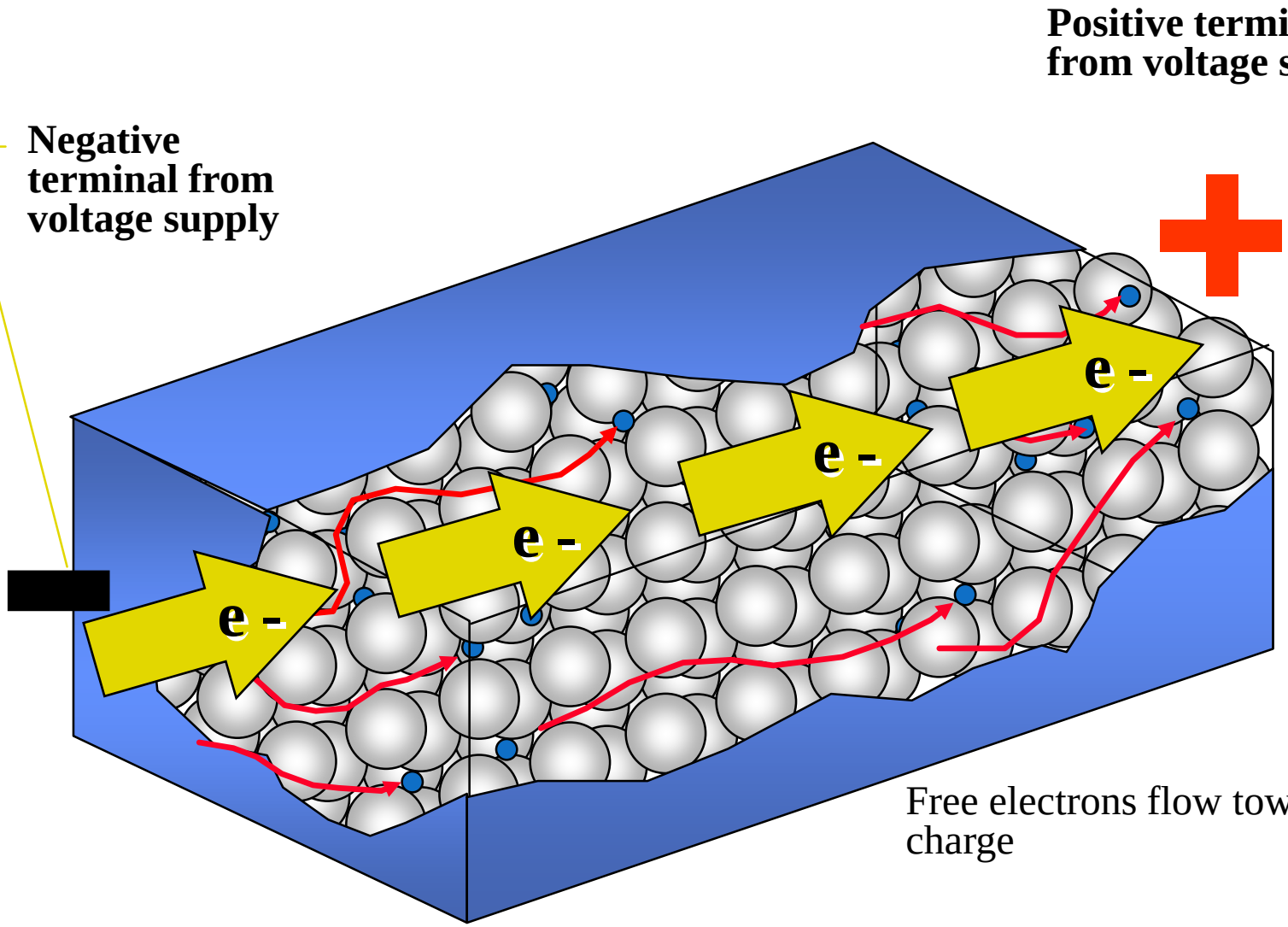
- E_d << Eg (band gap energy)
  - ✓Usually, For Si: Ed < 0.1 eV, Eg = 1.12 eV

- At room temperature, the thermal energy available is sufficient to excite large numbers of electrons from donor states (E_d) to the CB:
  - ✓Very few electron-hole pairs
  - ✓n >> p (electron is majority carrier)
  - ✓ Called n-type semiconductor

Flow of Electrons in Copper Wire

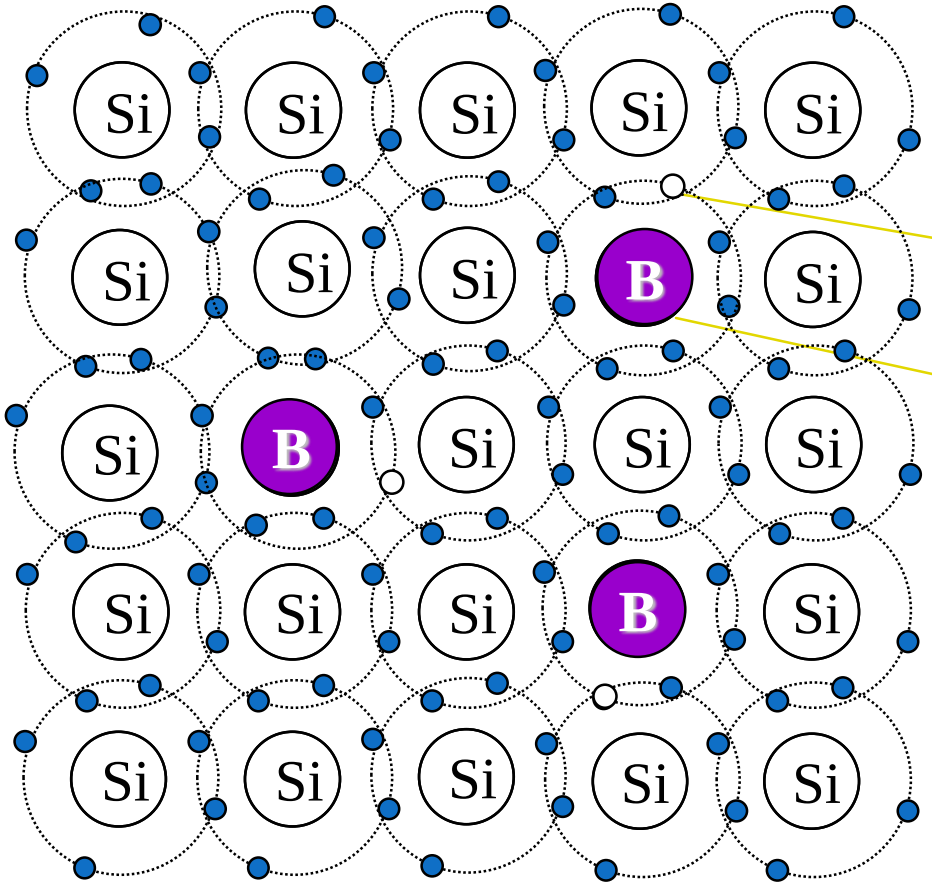


Flow of Free Electrons in N-type Si



Free electrons flow toward positive charge

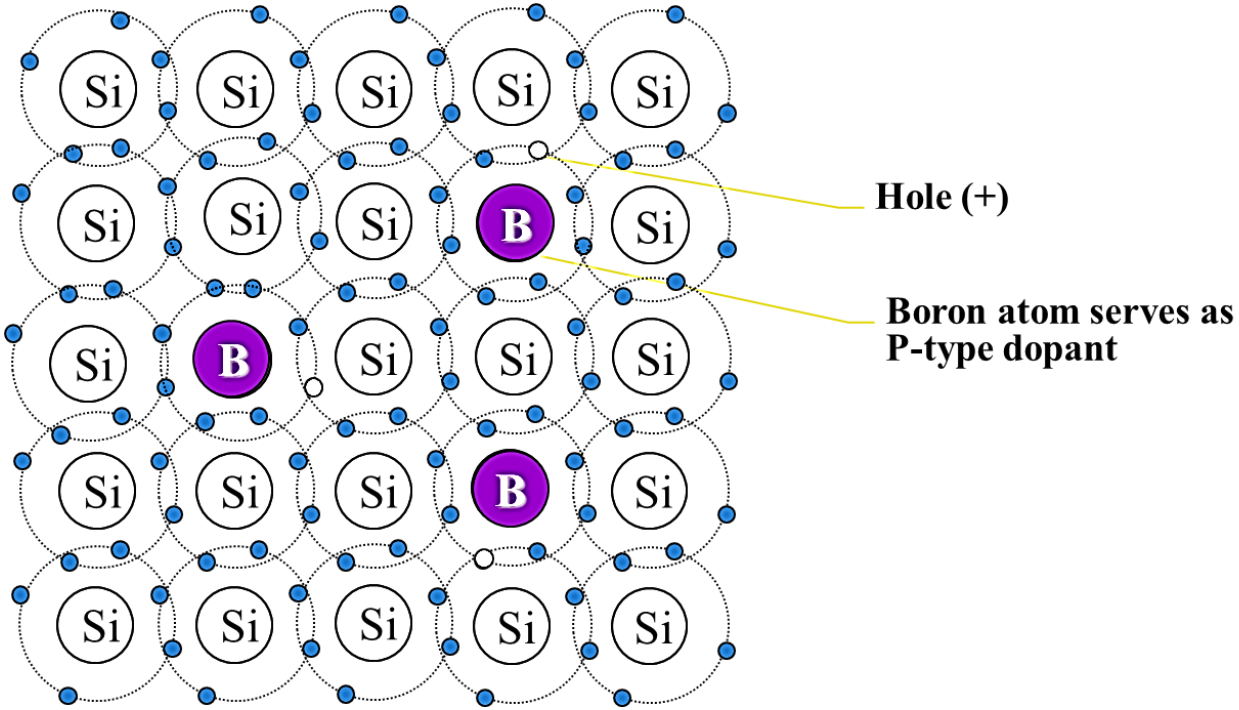
Free Holes (h^+) in P-type Si



Acceptor atoms provide a deficiency of electrons to form P-type silicon.

Free Holes in p-type Silicon

- A group IIIA (3A) element, such as B atom is added into Si. One of the covalent bonds around each dopant atom is deficient in an electron, leaves an empty hole that an electron can move into.
- Acceptor atoms provide excess holes to form P-type Si.



Free Holes in p-type Silicon

- Excess holes locate in a **acceptor state (E_a)** close to the bottom of the band gap. When an electron fills the acceptor state, a hole is left in the valence band
- Each excitation accept a electron to the conduction band; This type of dopant is called a ***acceptor.***

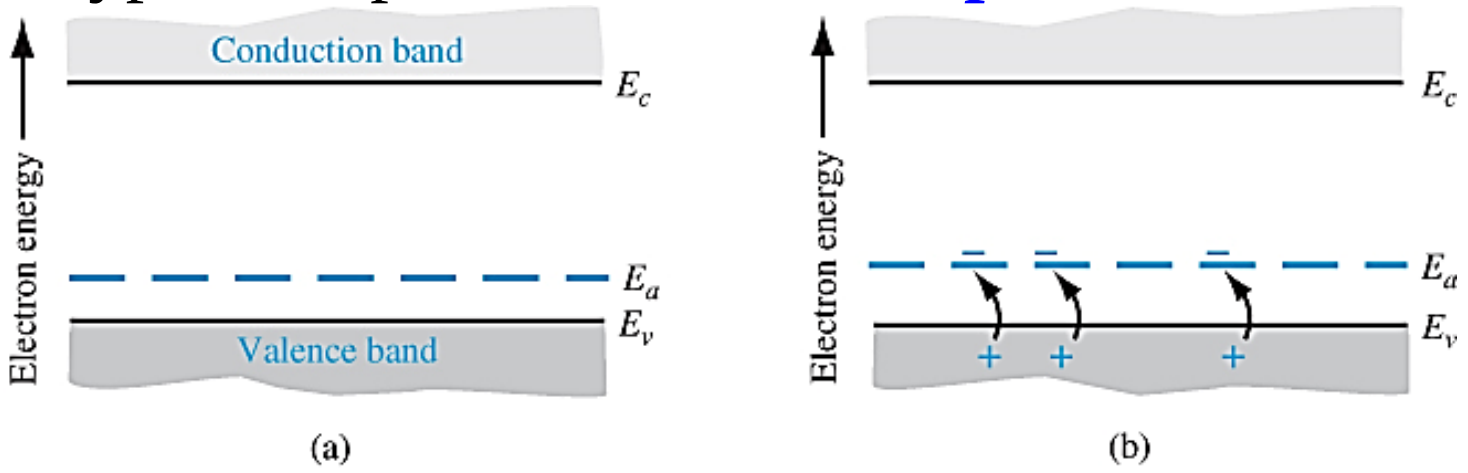


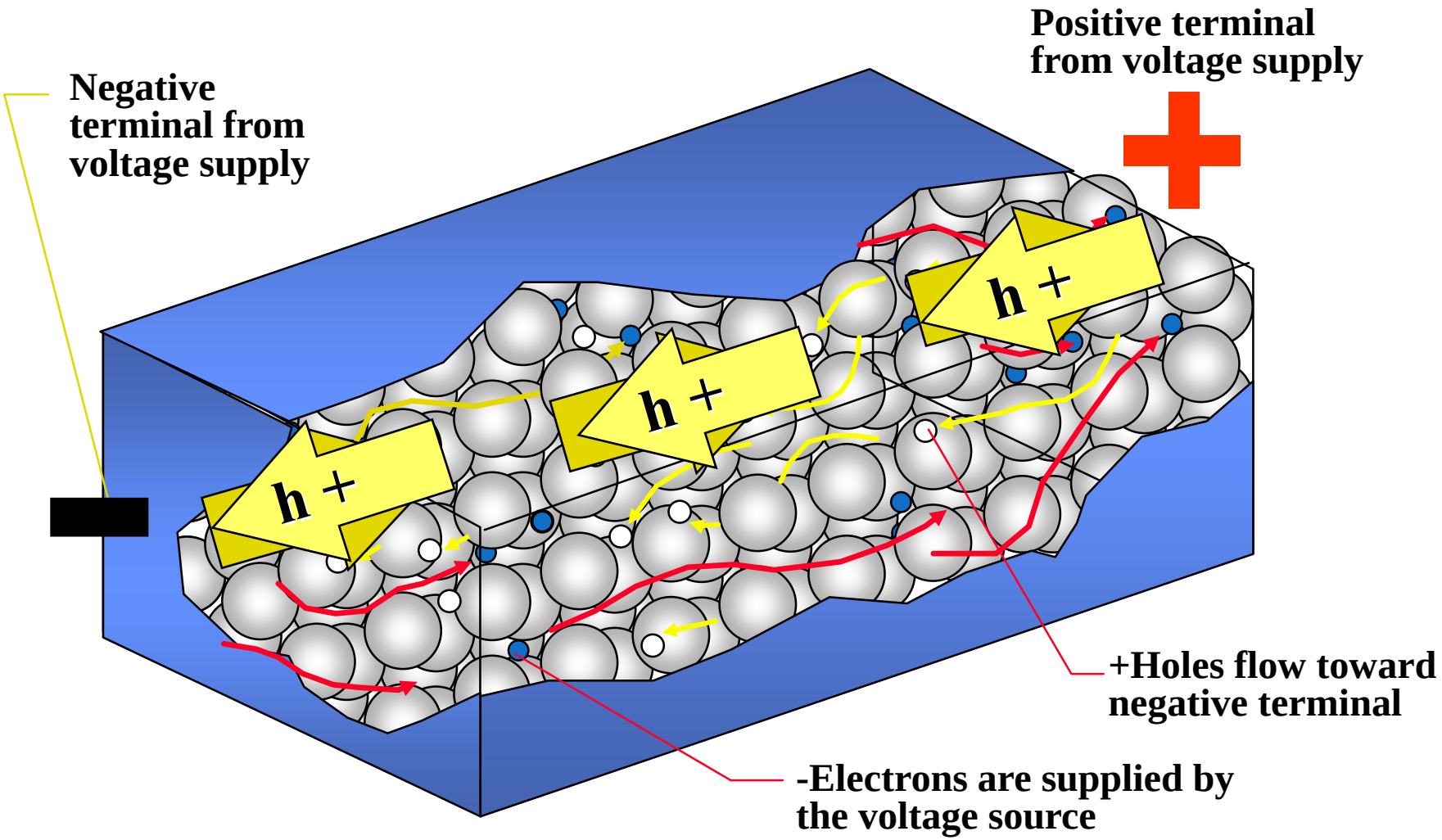
Figure 4.7 | The energy-band diagram showing (a) the discrete acceptor energy state and (b) the effect of an acceptor state being ionized.

p-Type Semiconductor

- E_A << Eg (band gap energy)
  - ✓Usually, For Si: E_a < 0.1 eV, Eg = 1.12 eV

- At room temperature, the thermal energy available is sufficient to excite large numbers of electrons from VB to the acceptor states (E_A):
  - ✓Very few electron-hole pairs
  - ✓p >> n (hole is majority carrier)
  - ✓ Called p-type semiconductor

Flow of Holes in P-type Si



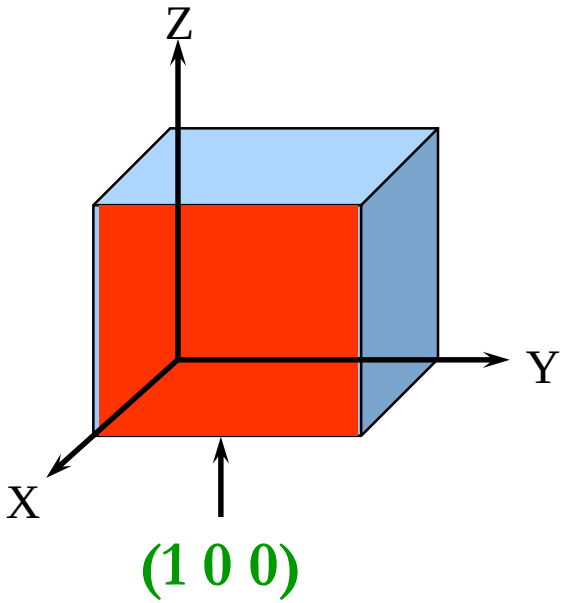
Outline

- Introduction to the Semiconductor
- How does Semiconductor Work?
- **Si Wafer Orientation**

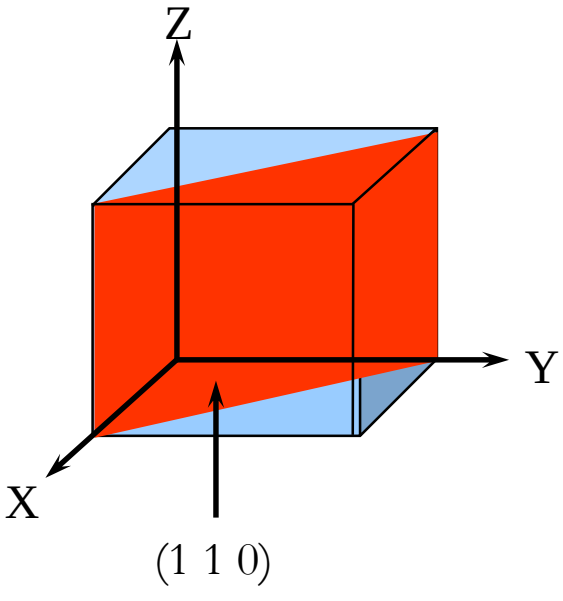
Miller Indices of Crystal Planes

Miller Indices **(**h k l**)** plane

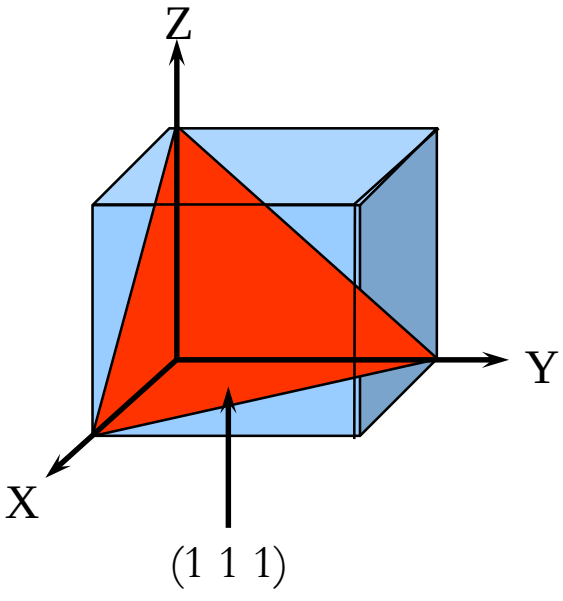
Equivalent planes {h k l}



(1 0 0)



(1 1 0)

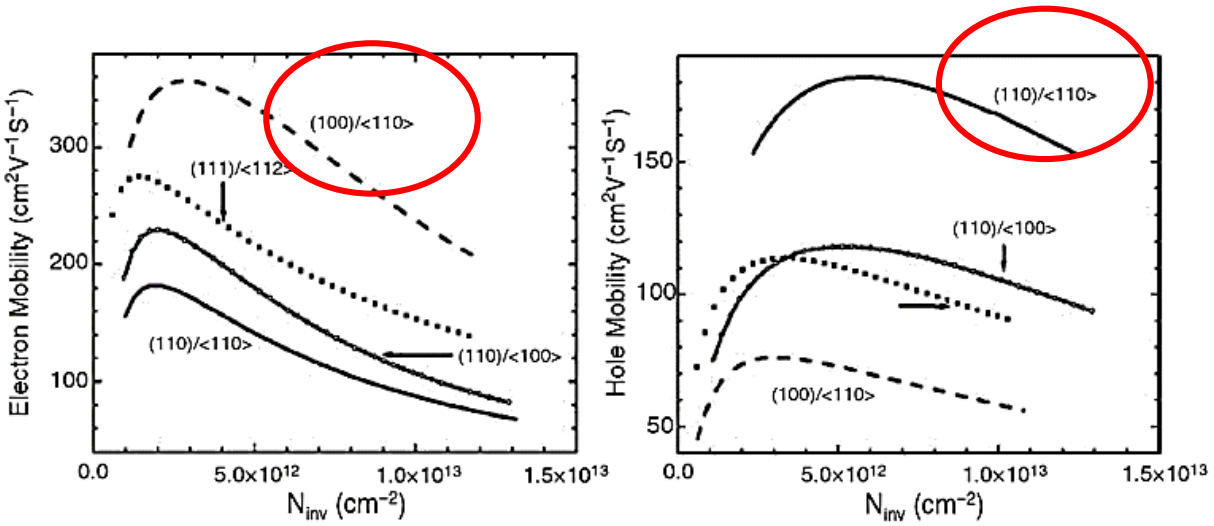


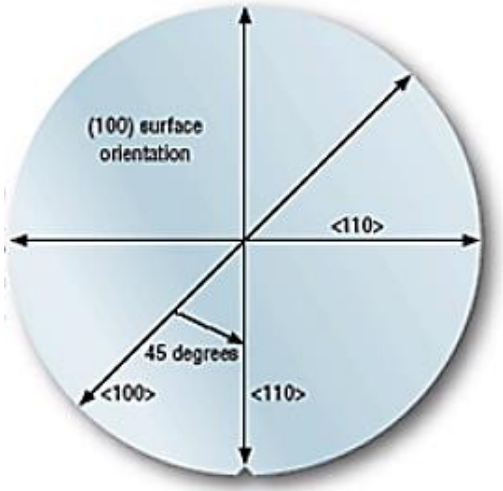
(1 1 1)

- Find the intercepts of the plane with x, y, and z axes. **(1 ∞ ∞)**
- Take the reciprocals of the intercepts **(1/1 1/∞ 1/∞)= (1 0 0)**
- Multiply the lowest common denominator **(1 0 0)**

(1 0 0) Si Wafer

- **CMOS** fabrication are typically used **(1 0 0) wafer** due to the low oxide/Si interface trap density and the highest electron mobility.
- For the NMOS, electrons have the highest mobility in the conventional (100) plane, and both [100] and [110] directions of the current flow are equivalent.



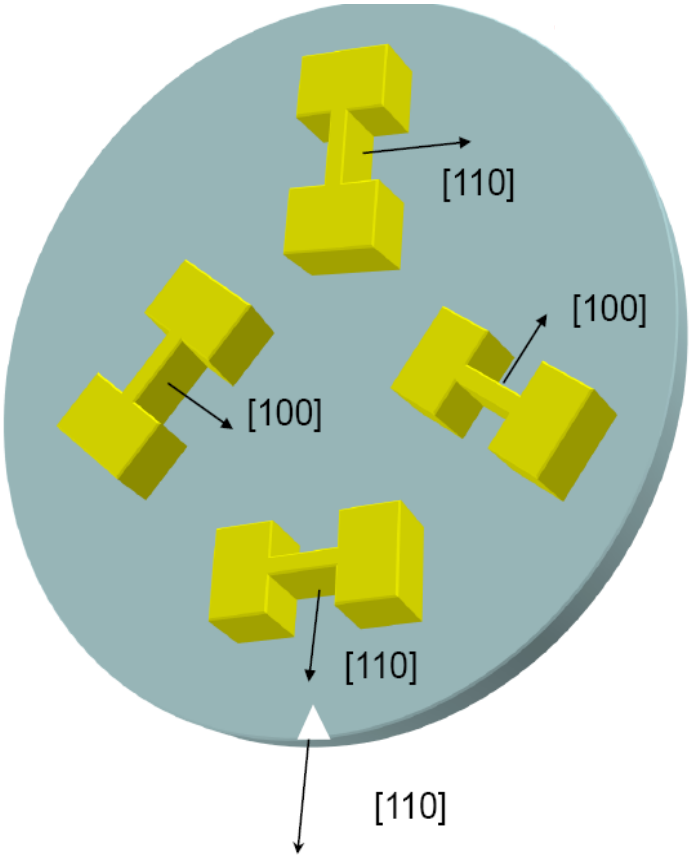


[1 1 0] Notch

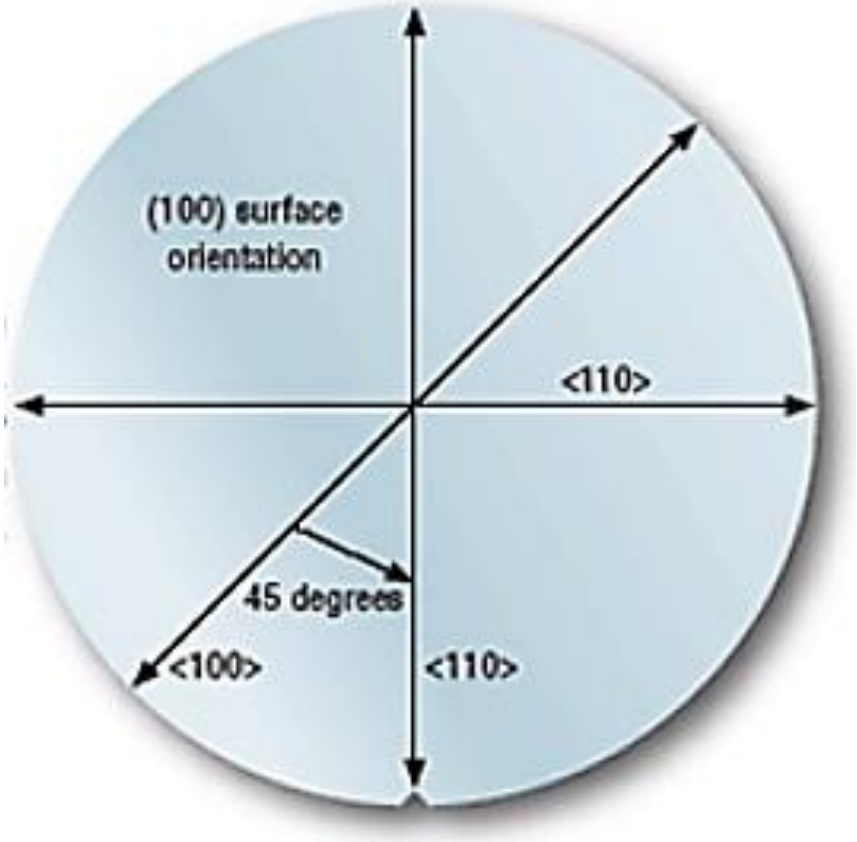
http://www.sunedisonsemi.com/index.php?view=100-notch

Orientation-Dependence Mobility

- Q1. Which transistors are located in the correct direction?

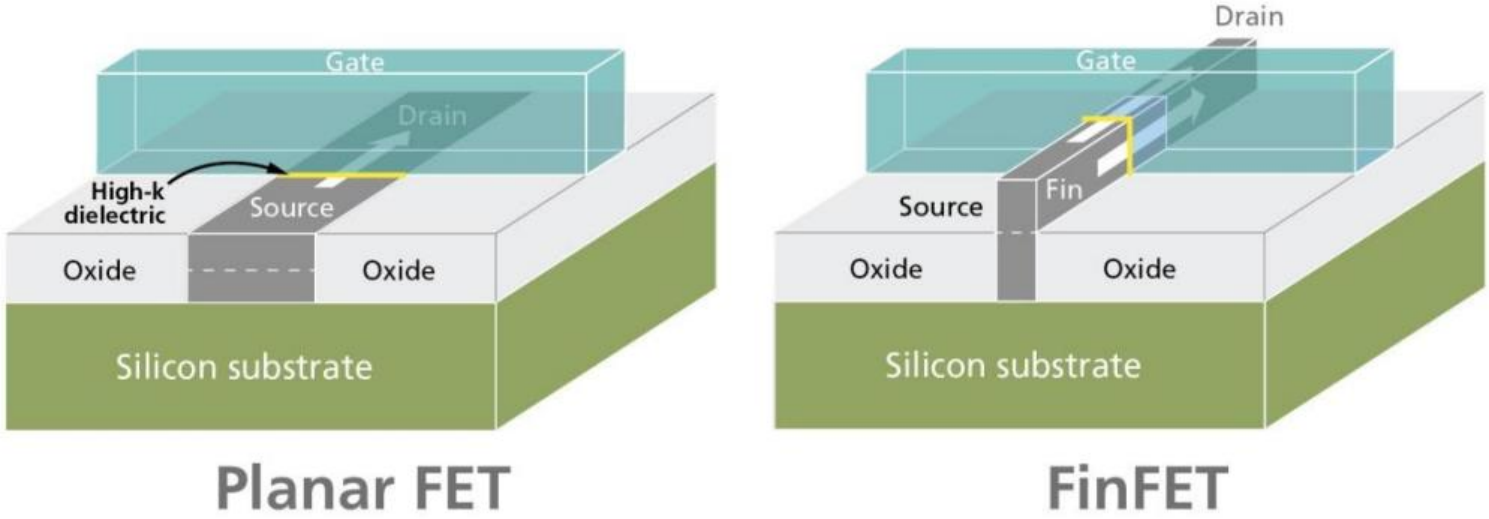


ED-2004, Vol. 51, No.10, p. 1621, 2004

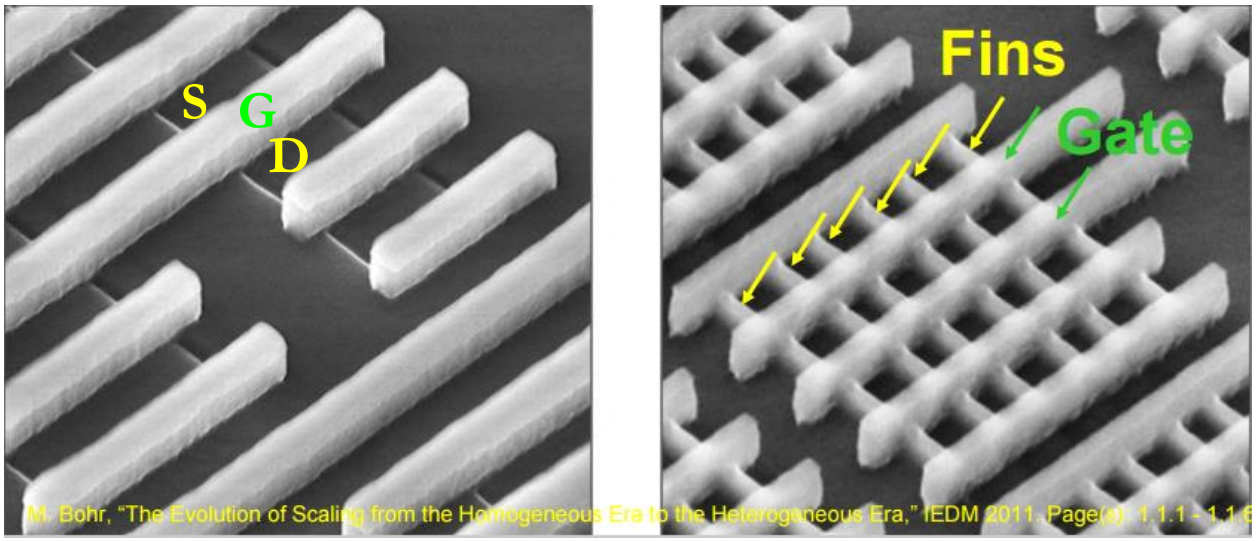


<1 1 0> Notch

2D & 3D Field Effect Transistor



Intel 32 nm
2D



Year: 2016
Intel 22 nm
3D

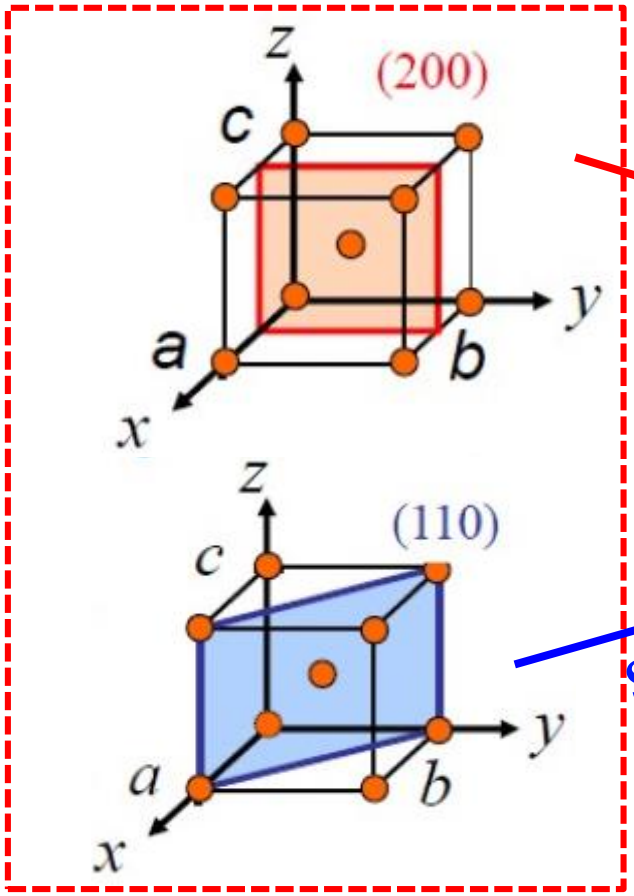
From: V. Singh, EUVL Workshop, 2014, Intel

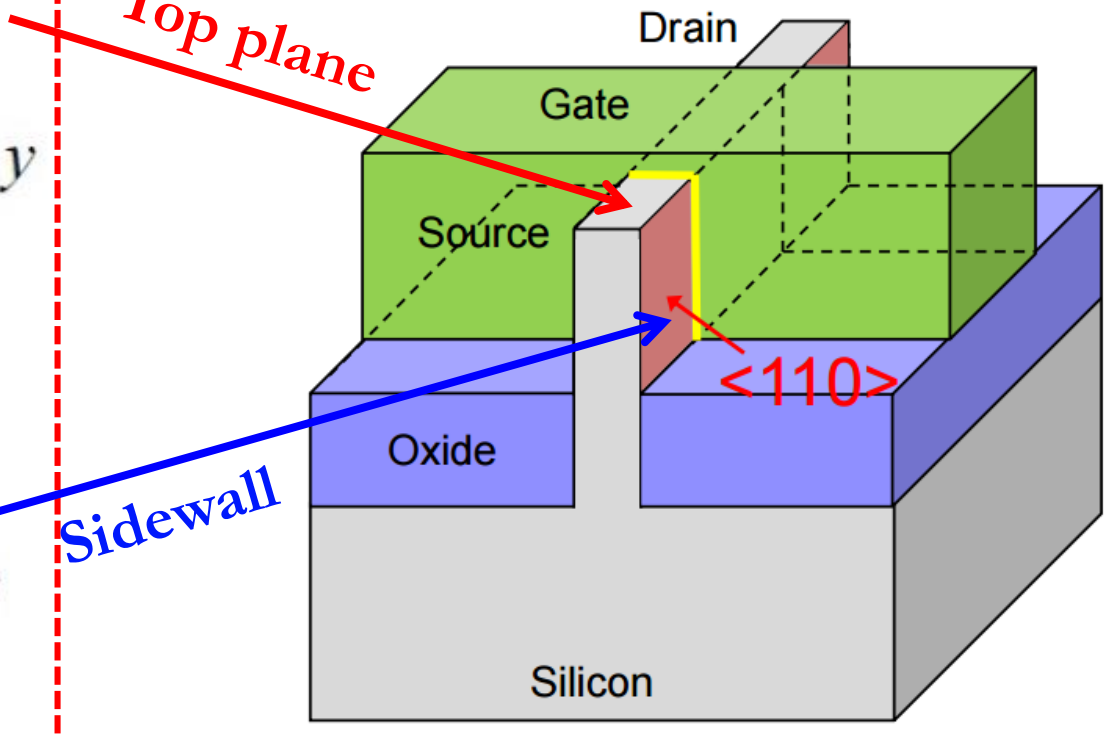
FinFET (3D Field Effect Transistor)

- Q1. Which plane is benefit for NMOS and PMOS, respectively?

- 網址參考:

https://www.youtube.com/watch?v=REWakvpXTxg

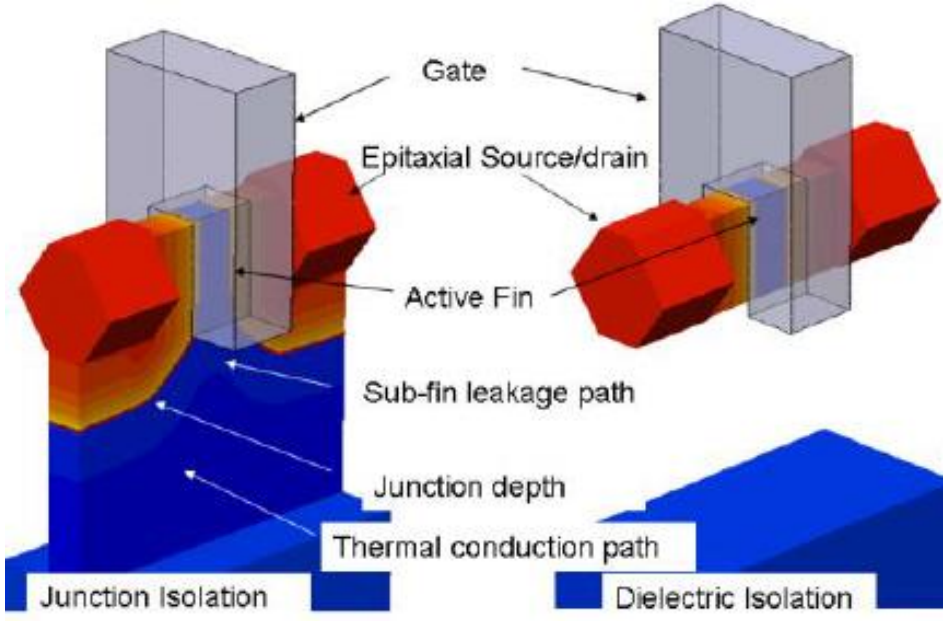


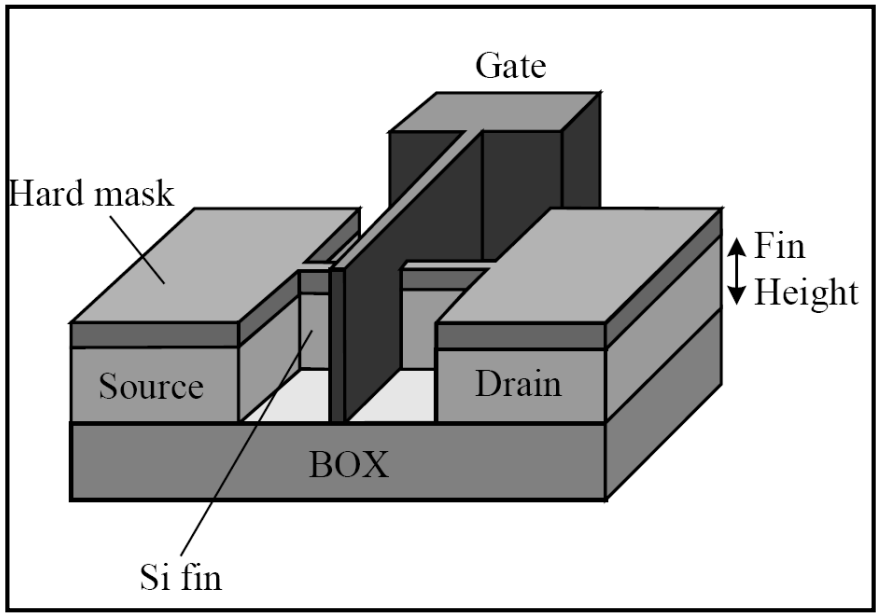


From: V. Singh, EUVL Workshop, 2014, Intel

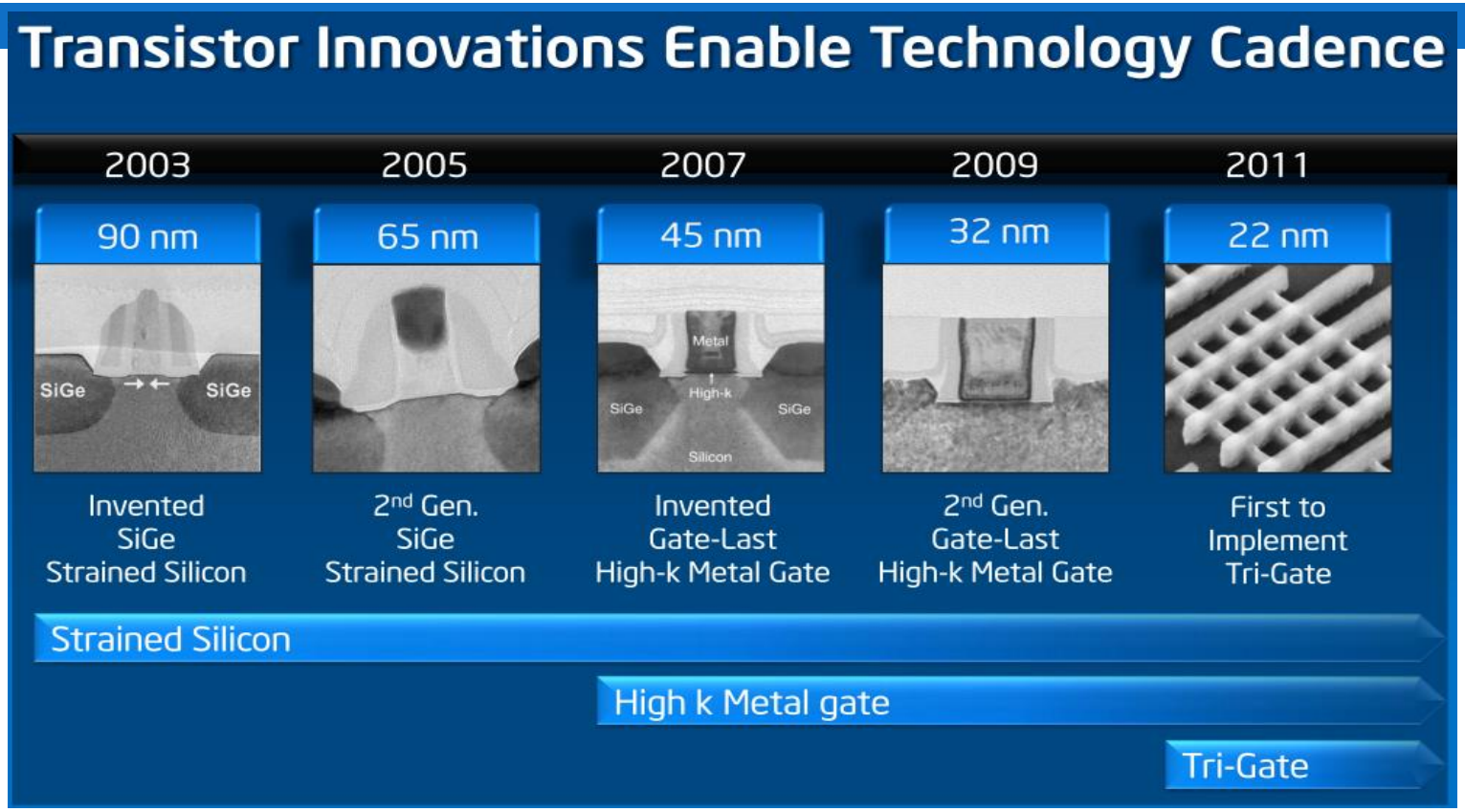
FinFET (3D Field Effect Transistor)

- Intel 22 nm device technology is based on 3D FinFET. The channel layer of this structural is a fin-shaped (Fin) silicon channel.
- When it is turned on, the current is parallel to the surface of the wafer. The gate is symmetrically sandwiched between the front and back of the channel, so that both ends of the channel are controlled by the gate.





Revolutionary Evolution of Transistor



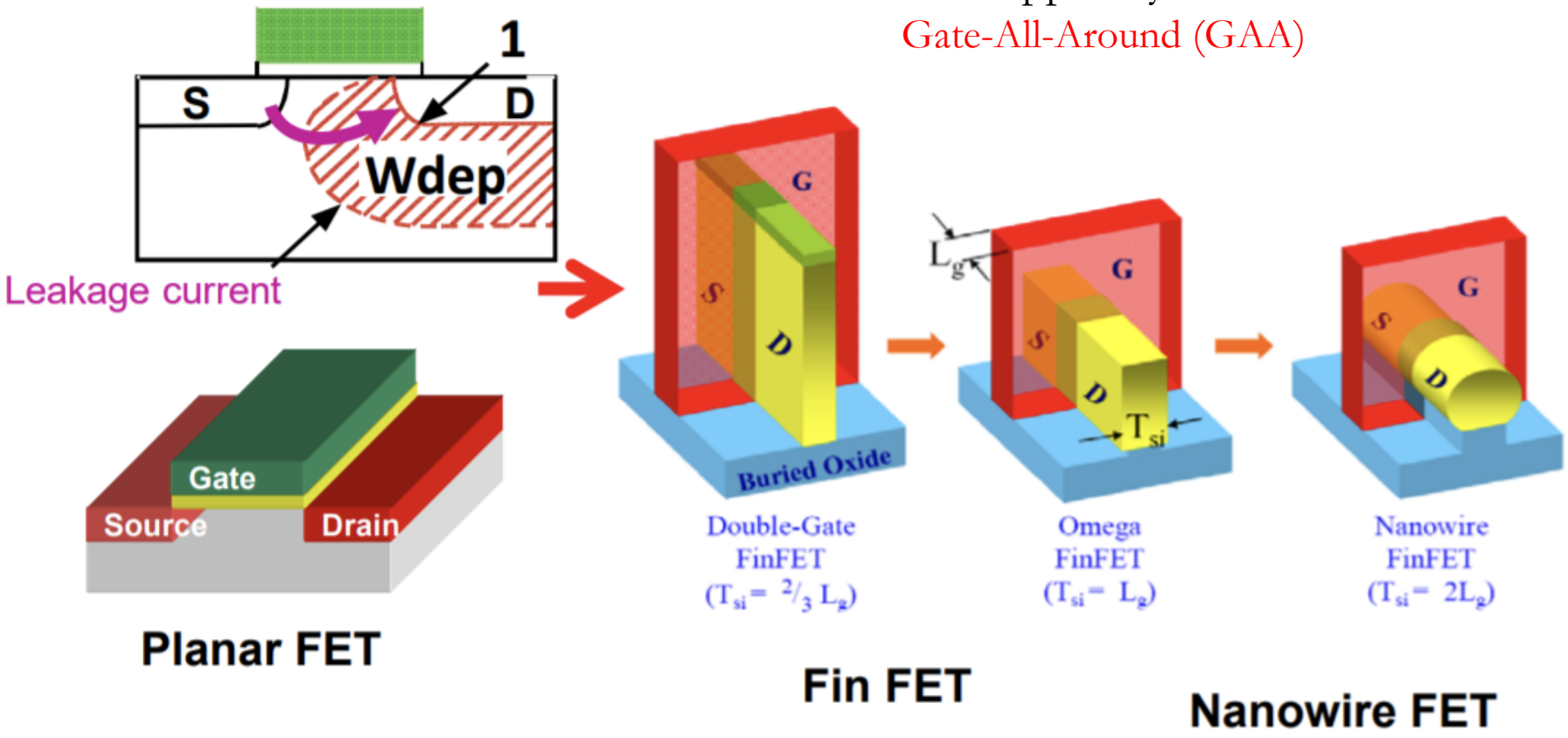
- Intel announces a major breakthrough in microchips: the world's first 3-D transistors in mass production. The transition to 3-D continues the pace of technology advancement, fueling Moore's Law for years to come.

Because of off-leakage control,

Planar → Fin → Nanowire

Channel is wrapped by Gate from all sides.

Gate-All-Around (GAA)



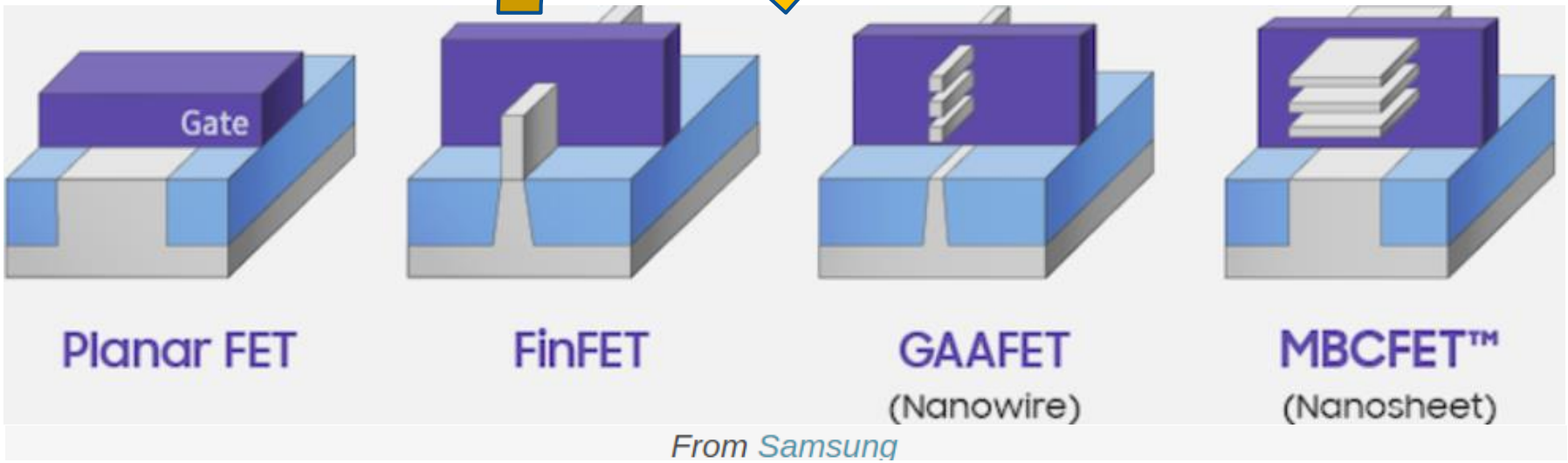
http://www.iwailab.ep.titech.ac.jp/pdf/201105ecs/iwai.pdf

Gate-All-Around Structure (Samsung)

- The Gate-All-Around (GAA) can be either really small (nanowire) or wider (nanosheet), with multiple stacked wires or sheets increasing the effective width of the transistor when it comes to drive current metrics.

5 nm → 3 nm

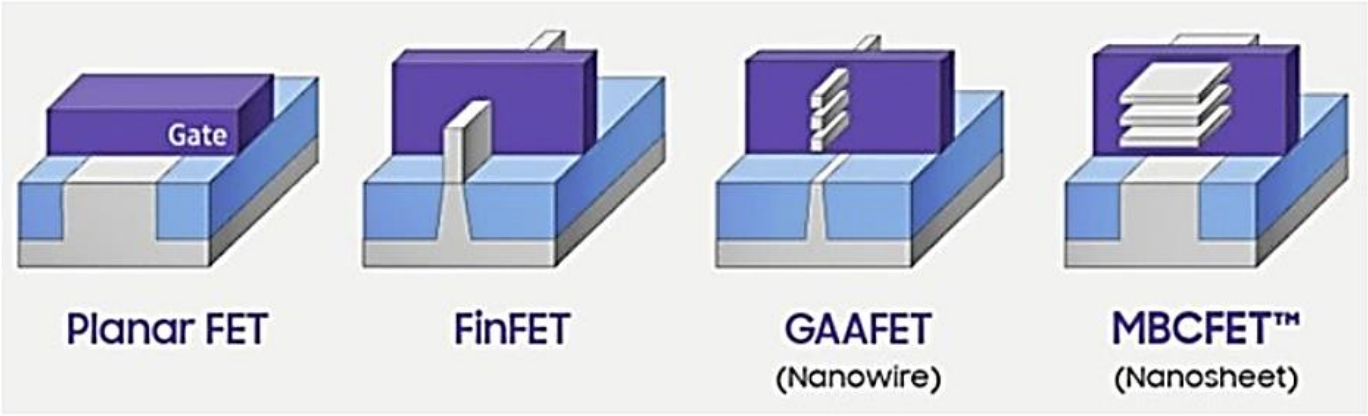
- Area reduction by ~35%
- Power consumption reduction by ~50%
- Computing performance increasing by 30%

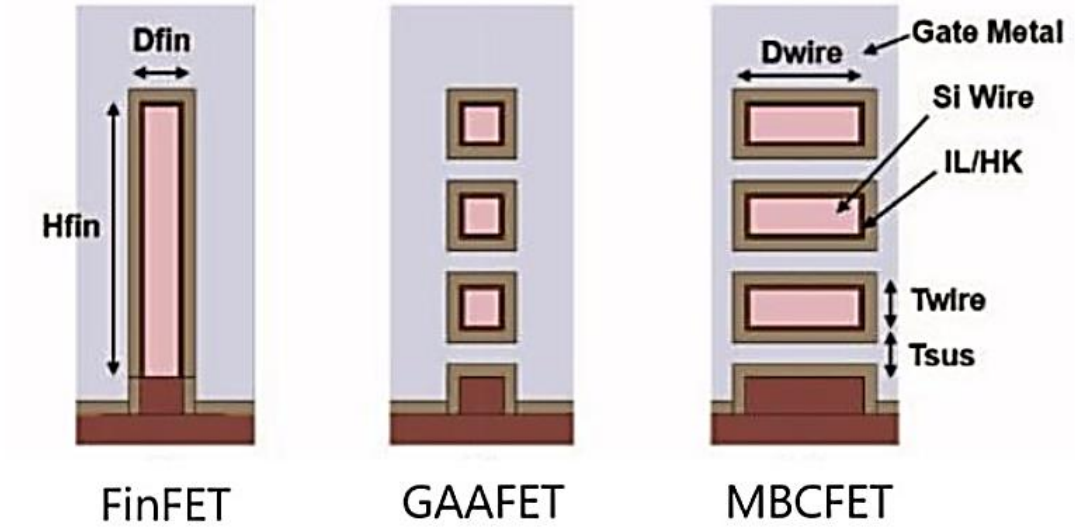


From Samsung

https://www.anandtech.com/show/15865/intel-to-use-nanowirenanoribbon-transistors-in-volume-in-five-years

Gate-All-Around Structure (Samsung)

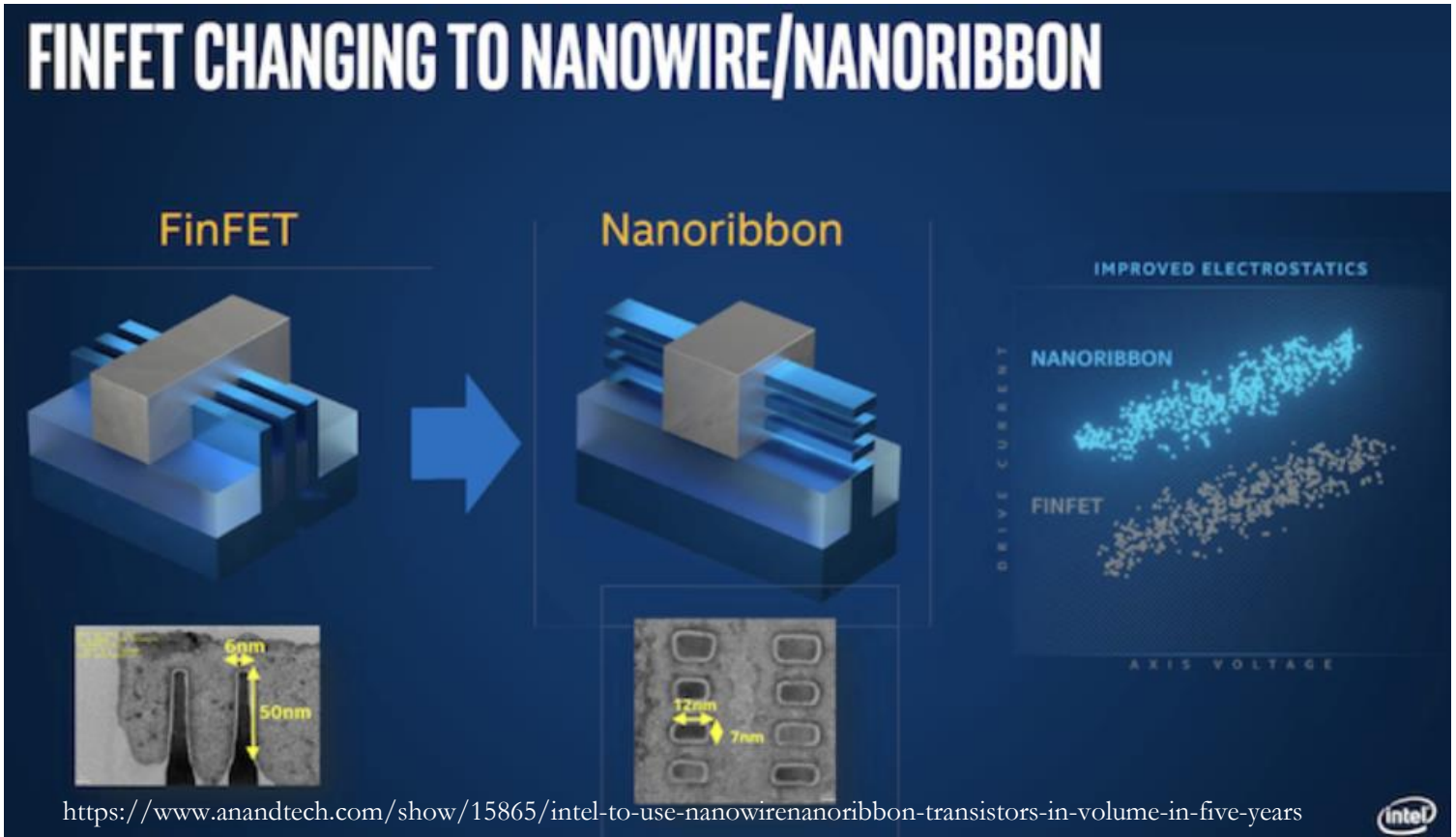




Cited from imec website

Gate-All-Around Structure (Intel)

- GAA is expected to implement for '3nm or 2nm' node for most foundry businesses, which should offer similar density to Intel's '5nm node'.



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