

Contents

List of Figures	ix
List of Tables	xi
Abbreviations and Acronyms	xiii
Abstract	xv
<i>Resumen</i>	<i>xvii</i>
<i>Resum</i>	<i>xix</i>
1 Introduction	1
1.1 Background	2
1.1.1 Memory Technologies	2
1.1.1.1 Static Random-Access Memory (SRAM)	2
1.1.1.2 Leakage Reduction Techniques for SRAM	3
1.1.1.3 Dynamic Random-Access Memory (DRAM)	3
1.1.1.4 Other Memory Technologies and Cells	5
1.1.2 Last-Level Caches	6
1.1.2.1 Replacement Algorithms	6
1.1.2.2 Refresh Mechanisms	8
1.2 Objectives of the Thesis	10
1.3 Contributions of the Thesis	11
1.4 Thesis Outline	12
2 Hybrid eDRAM/SRAM L1 Data Cache Architecture	13
2.1 Memory Cell Proposal	14
2.2 Architectural Design Issues	16
2.2.1 Accessing the eDRAM Ways	18
2.2.2 Increasing the Percentage of Hits in the SRAM Way	20
2.2.3 Devised Writeback Policies	22
2.3 Experimental Evaluation	23
2.3.1 Simulation Framework	23
2.3.2 Performance	25
2.3.2.1 SRAM and eDRAM Hit Ratio	25
2.3.2.2 Impact of eDRAM Access Time	26
2.3.2.3 Impact of Retention Time	28

2.3.2.4	Writeback Policies	29
2.3.3	Energy Consumption	31
2.3.3.1	Methodology	31
2.3.3.2	Energy Results	32
2.3.4	Area Savings	34
2.4	Summary	35
3	Hybrid eDRAM/SRAM L2 Cache Architecture	37
3.1	Motivation	38
3.2	Hybrid Last-Level Cache Design	40
3.2.1	Accessing the Hybrid Cache: Bank-Prediction	41
3.2.2	Keeping the Last Accessed Blocks in SRAM Banks	41
3.2.3	Distributed Refresh	43
3.3	Experimental Evaluation	44
3.3.1	Area	45
3.3.2	Performance	46
3.3.3	Energy Consumption	50
3.3.4	Energy-Delay Squared Product	53
3.3.5	Energy-Delay-Area Product	55
3.4	Contemporary Hybrid Architectures	57
3.5	Summary	58
4	MRU-Tour Replacement Algorithms	61
4.1	Weaknesses of LRU	62
4.2	MRUT Concept and MRUT-based Algorithms	63
4.2.1	Overview	63
4.2.2	MRUT-based Algorithms	64
4.3	MRUT Patterns	65
4.4	Experimental Evaluation	67
4.4.1	Performance of the Baseline MRUT	67
4.4.2	Enhancing MRUT Performance	68
4.4.3	Introducing the Victim Cache	73
4.4.4	Comparison Against Other Recent Approaches	76
4.5	Hardware Complexity	78
4.6	Reuse Information and Other Replacement Algorithms	80
4.7	Summary	82
5	Selective Refresh	85
5.1	Energy-Aware eDRAM and Hybrid Cache Architectures	86
5.1.1	Cache Hit Distribution and Bank-Prediction	86
5.1.2	Coupling the MRUT Algorithm with the Proposed Caches	87
5.1.3	Selective Refresh Policies	88
5.2	Experimental Evaluation	90
5.2.1	Energy Consumption	90
5.2.2	Performance	94
5.3	Refresh Mechanisms in Off-Chip Memories	97
5.4	Summary	98

6 Conclusions	101
6.1 Contributions	102
6.2 Future Directions	103
6.3 Publications	104
References	109